Jalpaiguri Government Engineering College

(An Autonomous Government College)

Jalpaiguri, West Bengal

Question Bank

Subject- Analog and Digital Electronics

Department- Computer Science and Engineering

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Topic: Boolean Algebra and Logic Simplification

1. What is Boolean Algebra? What is its utility in digital circuit design?
2. Explain different laws of Boolean Algebra.
3. Write DeMorgan's law/theorems. Write them in equation form. Prepare the truth table to prove their correctness.
4. How can AND-OR circuit be converted to NAND logic?
5. What is Karnaugh map? What is its utility? How is it drawn? Explain the procedure for grouping of cells in K-map.
6. What is logic race? What is meant by Don't care condition? Give example.
7. Use K-map to simplify the following
   a) Y=ABC+A'BC+AB'C'+AB'C+ABC'
   b) Y=ABCD+AB'CD+ABCD'+ABC'D+ABC'D'
   c) Y(A,B,C,D)=∑m(0,2,3,6,8,9,14,15)
   d) Y= ABC+ AB'C+A'BC+A'B'C
   e) Y=ABC'D'+BAC'D+ABCD'+AB'CD+ABCD
   f) F(A,B,C,D)=∏M(0,4,6,8,10,12,14)
   g) Y=A'B'C'D'+AB'C'D+A'B'CD+ABCD'+AB'CD'+A'B'C'D

Topic: Combinational Logic Circuits

1. What is combinational logic circuit? Write the main features of combinational logic circuit. Give some examples of combinational logic circuit.
2. What is the function of memory in digital circuits? Which circuit does not need memory? Why?
3. What are the differences between combinational and sequential logic circuits?
4. Discuss the procedure to design a combinational logic circuit.
5. Why is it necessary to simplify a Boolean expression before realizing the circuit ? How can the simplification be done?
6. Define half adder, full adder and adder-subtractor composite circuit. Design the circuits with any logic gate and or NAND gate only.
7. A logic circuit has four inputs, A,B,C,D. The output should be high when A is low and exactly two other inputs are low. Prepare a truth table. Obtain output expression. Draw the circuits with AND, OR logic gates.
8. A logic circuit has four inputs. The output is high only when three and only three inputs are high. Design the logic circuit.
9. A limited company has directors A, B, C, D holding 35%, 30%, 20%, 15% of the shares respectively. A major decision must have a support of minimum 60% of the stock. Design a combinational logic circuit for the voting in the company.
10. Design a combinational logic circuit so that output Y is equal to input A when control inputs B and C are same. If B and C are different, Y should be High.
11. Design a combinational logic circuit which gives High output when majority of inputs A,B,C is Low.
12. A combinational logic circuit has 3 inputs A, B, C and output F. F is true for following input combinations: a) A is false, B is true b) A is false, C is true c) A, B, C are true d) A, B, C are false. Now answer the following

    i) Write truth table for F. Use the convention true =1 and false =0

    ii) Write the simplified expression for F in SOP and POS form.

    iii) Draw the circuit with NAND gate.

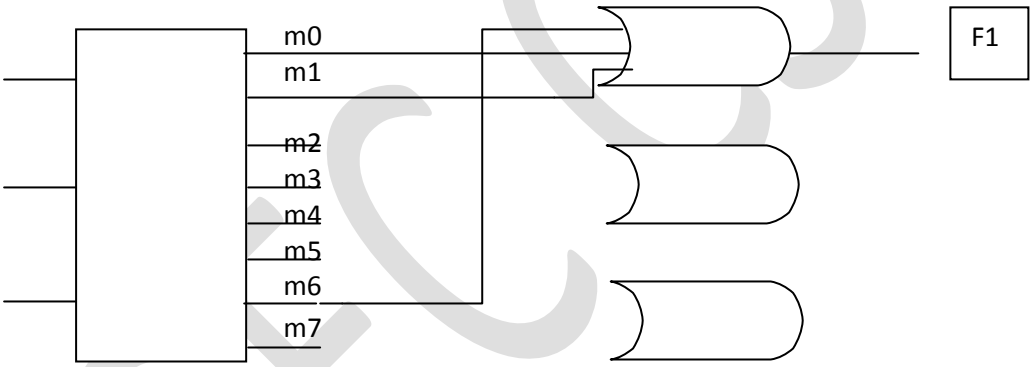
Topic: encoder, decoder, multiplexer

1. Define the following a) encoder, b) priority encoder, c) decoder
2. Draw the logic circuit of decimal to BCD Encoder and explain its working.
3. Draw a complete circuit of a 4 line to 16 line decoder.
4. A combinational circuit is defined by the following three functions: F1=x'y'+xyz', F2=x' +y, F3 = xy + x'y'. Design the circuit with a decoder and external gates.

   [F1=x'y'(z+z')+xyz'=x'y'z+x'y'z'+xyz'=m1+m0+m6

   F2 = m0+m1+m2+m3+m6+m7

   F3 = m0+m1+m6+m7]



5. Design a full adder using decoder circuit.
6. What is MUX? Use a MUX to generate the function f=AB+BC+AC
7. Use a 8:1 MUX to generate the function, f(A,B,C,D)=∑m(0, 1, 3, 5, 13, 14, 15).
8. Use a 8:1 MUX to generate the function
   a) F= A'B+AD'+CD+B'C'
   b) f(A,B,C,D)=∑m(0, 1, 3, 9, 10 , 12, 13, 15). Considering C is the data line
9. What is multiplexer tree? Write the application of multiplexer tree.
10. Implement a full adder circuit using decoder circuit and MUX circuit.

Topic: Flip flops

1. What is flip flop? Write the applications of flip flops.
2. Name some parameters of flip flops.
3. What is JK master slave flip flop? Draw its logic circuit, explain its working with truth table.
4. What is latch? How a latch is different from flip flop?
5. What is SR latch? Draw its logic circuit with a) NOR Gate b) NAND Gate, and explain its working.
6. What is excitation table of a flip flop? Why is it needed? State the excitation table of all flip flops.
7. What is race around condition/ what is the drawback of JK flip flop? How can we overcome it?
8. Convert a SR flip flop into JK flip flop. State the conversion table, conversion logical expression and circuit diagram.
9. Convert a JK flip flop into SR flip flop. State the conversion table, conversion logical expression and circuit diagram.
10. Convert a SR flip flop into D flip flop. State the conversion table, conversion logical expression and circuit diagram.

Topic: Shift Register

I. Write two functions of shift register.

II. Write the applications of shift register.

III. What is universal shift register (USR)? Draw the circuit and explain its working.

IV. Which flip flops are used in shift register?

V. Can a shift register be used as a counter? Explain.

VI. What is the disadvantage of serial data input?

VII. What is a tri-state shift register? Why is it needed?

VIII. Data 0101 is entered into 4 bit serial in parallel out shift register. Draw a diagram to show the states of registers after 1, 2, 3, 4 clock pulses.

IX. A 4 bit USR contents are 1101. Draw diagram to show register contents after a) 1 right shift, b) 2 right shift, c) one left shift, d) two right and one left.

X. In a PIPO register A=1, B=1, C=0, D=1. what are the data outputs after 3 clock pulses?

Topic : Counter

1. What is the function of a counter?
2. Which flip flops are used in counter?
3. What is meant by modulus of a counter?
4. Differentiate between asynchronous and synchronous counters.
5. Explain the terms: up counter, down counter up-down counter.
6. Name some application of counter.
7. Why is ripple counter so called? What is its special feature?
8. What is presettable counter?
9. What is decade counter?
10. What is ring counter? Draw its circuit and explain its working.
11. What is meant by cascading of counters? How is modulus affected by cascading?
12. How are counters classified?
13. Draw the circuit diagram of a 4 bit ripple counter. Explain its working. Draw the timing diagram.
14. Draw the circuit of a 4 bit up-down counter. How are both up and down features obtained?
15. What is the difference between ring and Johnson counter? Draw the circuit of four bit Johnson counter and explain its working. Draw the timing diagram of a 4 bit Johnson counter.
16. A ripple counter has 4 flip flops. The initial 3 states are to be skipped. Find the modulus. Draw the circuit.
17. Draw the circuit of a Mod-32 synchronous counter. How many logic gates are used in this device? [5 flip flops, 3 AND gates]
18. A ripple counter uses flip flops having tpd =14 ns. What can be the maximum modulus if the input clock frequency is 20 MHz. [Hints: T_{clock} >= Nxt_{pd} ; 1/(20x10^6)>=Nx14; 50>=Nx14]

19. In a synchronous counter with 4 flip flops, tpd of each flip flop is 40 ns and tpd of AND gate is 20 ns. Find the maximum possible frequency for which the counter can be used. [T_{clock} >=40+20 ns; max freq = $1/(60x10^{-9})$ =16.67 MHz]
20. A synchronous counter has 6 flip flops and 4 AND gates, t_{pd} of each flip flop is 30 ns and t_{pd} of AND gate is 15 ns. Find the maximum possible frequency for which the counter can be used. [22.22 MHz]
21. Find the maximum frequency of ripple counter having (a) 4 bits (b) 6 bits. Assume t_{pd} of each flip flop as 20 ns. [hints – 4 bits i.e., 4 flip flops, max freq=$1/(4*20*10^{-9})$ Hz=10^9 /(4*20*10^6) MHz = 12.5 MHz]
22. How many flip flops and AND gates are needed for Mod-64 synchronous counter? [2^6 = 64, flip flops= 6 no, Number of AND gates for synchronous counter = (number of flip flops – 2) = 6-2=4]